Nexperia PNX1700 connected media processor

Delivering high-quality digital video & audio content for the latest multimedia products

With twice the performance of the PNX1500 series, high-definition (HD) video decoding, and support for new media standards such as H.264 and MPEG-4, the Nexperia PNX1700 powers the latest popular media-based features in the newest generation of consumer and commercial products.

Key features

- 2X performance of previous Nexperia media processors
- Supports many popular digital video and audio formats
  - encodes and decodes H.264, WMV9, MPEG-4, MPEG-2, and DivX
  - decodes HD resolutions of MPEG-2 and DivX
  - encodes and decodes MP3 and AAC
  - decodes Dolby AC-3®
- Designed for media processing
  - Advanced, super-pipelined 32-bit 550-MHz TriMedia TM5250 CPU with powerful multimedia and floating point instructions
  - On-chip, independent, DMA units perform I/O, coprocessing, scaling, advanced de-interlacing and 2D graphics acceleration
- Pin compatible with PNX1500 series for existing design reuse
- Video output up to 1920 x 1080 60p
- Supports up to 256-MB DDR SDRAM memory system at rates up to 400 MHz (total memory bandwidth of 1.6 GB/s)
- Comprehensive software development environment enables application development entirely in C or C++

Applications

- IP set-top boxes
- Security digital video recorders (DVRs)
- Personal video recorders (PVRs)
- Digital media adapters

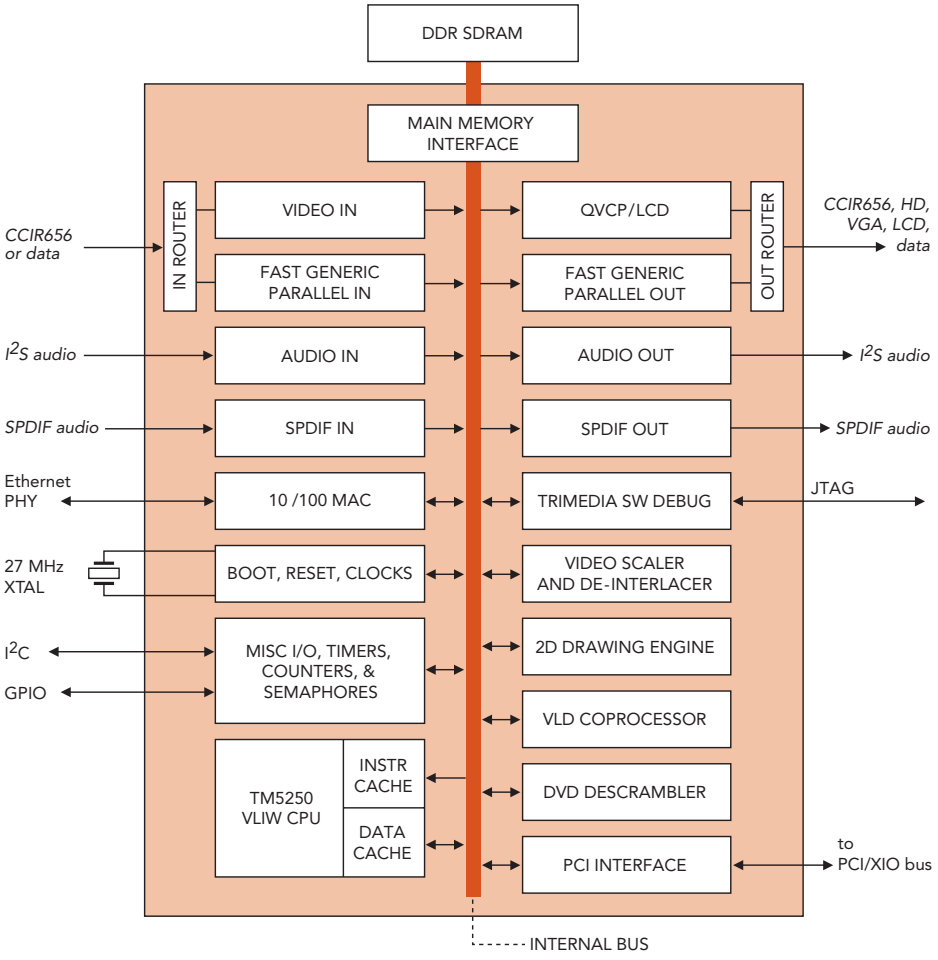
Continuing a tradition of low-cost, real-time connected media processors, the Nexperia PNX1700 handles popular video, audio, graphics, and communications standards such as H.264, Windows Media Technology, DivX, MPEG-2, MPEG-4, MP3, Dolby AC-3, TCP I/P, Ethernet, and Universal PnP. Doubling the performance of the PNX1500 series, the PNX1700 also decodes HD video formats including MPEG-2 720p and DivX-HD. Support for simultaneous encode and decode of MPEG-2 or MPEG-4 formats enables features such as watch-and-record and time-shift recording in PVRs. The PNX1700 maintains 100% pin compatibility with the PNX1500, ensuring design re-use and an instant performance boost for existing PNX1500 designs.

NXP founded by Philips

The PNX1700 features a TriMedia TM5250 CPU core with an enhanced set of powerful multimedia and floating point instructions. On-chip I/O and co-processing units perform high-quality hardware image scaling, advanced de-interlacing, picture enhancements, and complex 2D graphics acceleration. A TFT LCD controller and an Ethernet 10/100 MAC reduce the bill of materials and support advanced product configurations. Together the CPU and on-chip peripheral units make PNX1700 an ideal single-chip solution for delivering exceptional picture quality in a variety of connected multimedia appliances such as digital media adapters, IP STBs, security digital video recorders, and more.

The PNX1700 is supported by a comprehensive software development environment, enabling application development entirely in the C or C++ programming languages. Extensive application libraries, developed by NXP Semiconductors and third parties, improve time-to-market, reduce design cycles, and lower product development costs.

On a single chip, the Nexperia PNX1700 accelerates processing of audio, video, graphics, control, and communications datastreams.



Architectural overview

The PNX1700 leverages a powerful C/C++-programmable TriMedia CPU running a small real-time operating system to deliver efficient, predictable response to real-time events. Independent, on-chip, bus-mastering DMA units capture and format datastream I/O and accelerate processing of multimedia algorithms. A sophisticated memory hierarchy manages internal I/O and streamlines access to external memory. The result is a powerful, programmable media processor proven in standalone and hosted multimedia products.

C/C++-programmable VLIW CPU

The PNX1700 TriMedia TM5250 CPU core achieves top performance through an elegant implementation of a fine-grain parallel very-long instruction word (VLIW) architecture. It offers an extended instruction set that accelerates algorithms such as H.264 and WMV9 decode. The CPU enhances the performance of PNX1500 applications after only source recompilation. Additional performance gains can be achieved by leveraging the new TM5250 instructions.

The CPU's five issue slots enable up to five simultaneous RISC-like operations to be scheduled into only one VLIW instruction. These operations can simultaneously target any five of the CPU's 30 pipelined functional units within one clock cycle.

Enhanced instruction set

In addition to a full complement of traditional 32-bit integer and IEEE-754 compliant floating-point microprocessor operations, the TM5250 instruction set includes an extensive set of custom multimedia operations and single instruction multiple data (SIMD)-style operations (ops) for single 32-bit, dual 16-bit or quad 8-bit packed data. By combining multiple simple operations, a single custom op can implement up to 12 traditional microprocessor operations. In this way, up to 40 traditional operations can be executed in a single VLIW instruction. When incorporated into source code, custom ops can dramatically improve performance by taking advantage of the TM5250's highly parallel implementation.

On-chip I/O and co-processing units

Video input processor (VIP)

The VIP unit captures and processes digital video for use by on-chip units. It accepts up to 10-bit parallel YUV 4:2:2 digital video from any device or component that outputs a CCIR656-compliant stream or a YUV stream with separate horizontal and vertical syncs. During capture of a continuous video stream, the VIP unit can crop, horizontally downscale, or convert the YUV video to one of many standard pixel formats as needed before writing data to memory. When streaming video from TV broadcasts, it can also capture raw VBI data into a separate window in memory. This unit shares its pin interface with a fast generic parallel input unit through an input router.

Fast generic parallel input (FGPI)

The FGPI unit captures unstructured, infinite parallel datastreams, messages, or control signals — any datastream with no YUV processing requirements. When raw mode is enabled, an 8-, 16-, or 32-bit parallel datastream is captured continuously and double buffered into memory to receive, for example, an ATSC transport stream from an external channel decoder.

Video scaler and de-interlacer

A versatile, programmable memory-based scaler unit applies a wide variety of image size, color, and format manipulations to improve video quality and prepare it for display. The unit handles de-interlacing (with optional edge detection/correction), horizontal and vertical scaling, linear and non-linear aspect ratio conversions, anti-flicker filtering, pixel format conversions, and more.

Quality video composition processor (QVCP)

The QVCP unit composites two planes of display data from different sources before output. It supports either two video planes or one video plane and one graphics plane, such as video from DVD playback and graphics from a web browser. The QVCP unit works together with the on-chip 2D graphics engine and the memory-based scaler unit to support many types of multimedia applications at high speeds with few external components.

In addition to two-layer video compositing, the QVCP unit integrates scaling, a TFT LCD controller and many video quality enhancements including de-indexing or gamma equalization, contrast and brightness control, luminance sharpening, horizontal dynamic peaking, skin tone correction, dithering, and screen timing generation for the target display.

QVCP outputs the resulting video datastream to any of a wide variety of off-chip video subsystems supporting CCIR656, YUV, or RGB formats, progressive or interlaced scan modes, and resolutions up to 1920 x 1080 60p. It shares its pin interface with the fast generic parallel output unit through an output data router.

Fast generic parallel output (FPGO)

The FPGO unit outputs any raw datastream with no video post processing requirements, such as an ATSC bitstream. It can also broadcast unidirectional messages to other PNX1700 processors.

Audio input (AI) and audio output (AO)

Highly programmable AI and AO units provide all signals needed to read and write digital audio datastreams from/to most high-quality, low-cost serial audio over-sampling A/D and D/A converters and codecs. Both units connect to off-chip stereo converters through flexible bit-serial I²S interfaces. Their high level of programmability provides tremendous flexibility in handling custom datastreams, adapting to custom protocols, and upgrading to future audio standards.

The AI unit supports capture of up to eight channels of stereo audio. In raw mode, it captures any quantity of bits from the programmable frame.

The AO unit outputs up to eight channels and directly drives up to four external stereo I²S or similar D/A converters or highly integrated PC codecs. Software support for decoding Dolby AC-3 is provided through optional application library modules.

S/PDIF input and output

An S/PDIF (Sony/Philips Digital Interface) input unit connects to external sources of digital audio, such as a DVD player, to receive audio streams a variety of formats, including stereo PCM data, 5.1-channel Dolby AC-3 data (per IEC-1937), and more. An S/PDIF output unit outputs a high-speed serial datastream. Primarily used to transmit digital S/PDIF-formatted audio data to external audio equipment, it can also be used to output two-channel linear PCM audio from an internal audio mix or captured, compressed multi-channel audio streams such as Dolby AC-3 or AAC (per Project 1937). Software-decoded audio can be mixed with other audio before output.

Both S/PDIF input and output units have independent, programmable sample rates guaranteeing synchronization to any system time reference. Datastream content is software generated and controlled.

2D drawing engine (2D DE)

An on-chip 2D rendering and DMA engine accelerates high-speed 2D graphics operations including solid fills, lines, three-operand bitblts, and color expansion of monochrome data to any supported pixel format. A full 256-level alpha bitblt blends source and destination images together.

Variable length decoder (VLD)

A VLD coprocessor offloads the CPU during decoding or transcoding of Huffman-encoded MPEG-2 and MPEG-1 datastreams. It outputs to memory a decoded stream optimized for MPEG decompression software.

DVD descrambler

An on-chip DVD descrambler unit handles DVD authentication and descrambling tasks, enabling PNX1700 to integrate complete DVD datastream playback. An IDE DVD drive can be attached directly to the PCI/XIO interface.

Memory system

The PNX1700 couples main memory to substantial on-chip caches through a glueless main memory interface and internal bus system.

Glueless main memory interface (MMI)

The MMI acts as the main memory controller and programmable central arbiter, allocating memory bandwidth for on-chip unit activities. The MMI provides a 16- or 32-bit DDR SDRAM interface. The 32-bit interface is equivalent to a 64-bit SDR SDRAM interface running at 200 MHz, resulting in theoretical maximum bandwidth of up to 1.6 GB/s.

Programmable memory timing parameters enable the MMI memory controller to support most DDR SDRAM devices. Memory clock speed is programmable and independent of the PNX1700 CPU clock, eliminating the top-speed limitations of fixed memory/CPU clock ratios. Flexible memory configurations from 8 to 256 MB enable a variety of products to be built.

Dedicated instruction and data caches

The CPU is supported by separate, dedicated on-chip data and instruction caches employing a variety of techniques to improve cache hit ratios and CPU performance. A 16-KB L1, four-way, set-associative data cache supports a copy-back write and allocate on write policy, thus cache misses and CPU cache accesses can be handled simultaneously. Additional early restart techniques reduce read-miss latency. A 128-KB L2, eight-way, set-associative data cache further reduces the CPU stall cycles by prefetching and holding relevant data before the L1 data cache misses.

A 64 KB 8-way set-associative instruction cache provides several hundreds of bits of instructions every clock cycle. Instructions in main memory and cache use a compressed format to reduce internal bus bandwidth requirements.

High-speed internal bus

The PNX1700 CPU and processing units access external memory through an internal bus system comprising separate 64-bit data and 32-bit address buses. Arbitrated by the MMI unit, the internal buses maintain real-time responsiveness in a variety of applications.

PCI/XIO bus interface

A PCI/XIO interface connects the CPU and on-chip units to a variety of board-level memory components and off-chip devices. It allows simultaneous connection of 32-bit PCI master/slave devices as well as separate address/data-style 8- and 16-bit microprocessor slave peripherals, standard (NOR) or disk-type (NAND) Flash memories, or an IDE hard disk interface.

Control and connectivity

The PNX1700's versatile interfaces and control options support many advanced product configurations.

I²C interface

An I²C master/slave external interface operates in both standard (100 kHz) and fast (400 kHz) modes. It can connect to an optional EEPROM for boot and can be used to control a variety of I²C board-level devices.

Timers

Eight 32-bit general-purpose timers can be used for performance analysis, real-time interrupt generation and/or system event counting.

10/100 Ethernet MAC

The PNX1700 incorporates an Ethernet MAC sub-layer of the IEEE 802.3 standard, enabling an external PHY chip to be attached through a standard media independent interface (MII) or reduced MII interface (RMII). It implements dual-transmit descriptor buffers, supporting both real-time and non-real-time traffic. Quality of service (QoS) is ensured through low- and high-priority transmit queues.

TriMedia software debug (TMDBG) unit and JTAG port

The TriMedia interactive source debugger enables remote debugging of software running on the CPU core. A JTAG port connects a PC (running the debugger) to the TMDBG unit, enabling full support for interactive debugging features. The JTAG port is also used for boundary scan.

General purpose I/O (GPIO) and flexible serial interface

The PNX1700 supports 16 dedicated GPIO I/O pins for software I/O, external interrupt input, universal remote control (RC) blaster transmission, and signal sampling and pattern generation for emulating high-speed serial protocols.

IR remote control, receive and transmit

The PNX1700 uses the GPIO pin event sequence time-stamping mechanism and software event interpretation to execute RC commands. This approach supports a wide variety of RC protocols including Philips RC-5, RC-6, and RC-MM.

Dynamic power management

PNX1700 enables devices to conserve power by tailoring frequency to application requirements. Its software-programmable clocks enable the CPU to run at lower speeds, reducing power consumption during less cycle-consuming tasks. For example, decoding an MP3 audio stream requires less than 30 MHz of CPU cycles. Power is conserved by adjusting the clock speed on the fly to service this lower cycle requirement.

PNX1700 offers the ability to shutdown the CPU clock anytime the CPU is idle. In addition, each co-processing unit can be powered down by removing the clock, thereby providing additional power savings when the unit is not being used.

Robust software development environment

The PNX1700 is supported by a full suite of system software tools to compile and debug code, analyze and optimize performance, and simulate execution of its TriMedia CPU core. This comprehensive software development environment dramatically lowers development costs and reduces time-to-market by enabling development of multimedia applications entirely in the C and C++ programming languages.

Nexperia PNX1700 processors preserve investments in software development through compatibility between PNX1700 family members at the source code level. Powerful, optimizing compilers ensure that programmers never need to resort to non-portable assembler programming. As evolutionary hardware and software enhancements are incorporated into newer PNX media processors, increased performance can be achieved by simply recompiling application software.

TriMedia application libraries

Many application libraries are available from Philips and third-party suppliers. These C-callable routines are optimized for top performance on the TriMedia CPU and include modules for functions such as:

- H.264 encode/decode
- MPEG-4 (SP, MVP, ASP) encode/decode
- MPEG-2 encode/decode
- MPEG-1 encode/decode
- WMV9 decode
- MPEG-2 720p decode
- DivX-HD decode
- DivX-3, -4, -5, -6 decode
- DV decode
- H.32x encode/decode
- H.263 encode/decode
- Dolby AC-3 decode
- MP3 encode/decode
- AAC encode/decode
- TCP/IP, Ethernet, Universal PnP protocols
- more.

Specifications

Physical

Process	0.13-µm CMOS
Package	456 BGA
Power suppy	*core* 1.3V and 1.4V *DDR* 2.5 V *I/O* 3.3 V (5 V tolerant)
Power consumption	2 W typical at 450 MHz
Case temp.	0 to 85°C

Central processing unit

Type	TriMedia TM5250
Clock speeds	400 MHz, 450 MHz, 500 MHz, 550 MHz
Issue slots	5
Address space	32-bit, linear
Instruction set	Arithmetic and logical, load/store, custom multimedia and DSP, IEEE-754 compliant floating point
Data types	Boolean, 8-, 16- and 32-bit signed and unsigned integer, 32-bit IEEE floats
Functional units	30 pipelined: integer and floating-point arithmetic units, data-parallel DSP-like units
Registers	128 fully general purpose, 32 bits wide, non-banked
Interrupts	64 auto-vectoring, 8 programmable priority levels
Byte order	Big or little endian

Caches

Access	data 8-, 16-, or 32-bit words instruction 128 bytes
Associativity	4- and 8-way set-associative with hierarchical LRU replacement
Block size	64 bytes, 128 bytes
Size	L1 instruction cache 64 KB L1 data cache 16 KB; L2 data cache 128 KB

Video input processor unit (VIP)

External interface	36 pins: 32 data, 2 clock, and 2 validity signals
Formats	CCIR 601/656: 10-bit video (up to 40.5 Mpix/sec); HD video (using 20-bit YUV input mode)
Clock rate	Up to 81 MHz pixel clock
Functions	Programmable on-the-fly horizontal scaling
VBI formats	Closed Captioning, Teletext, NABST, CGMS, and WSS

Fast generic parallel input unit (FGPI)

Data rate	Up to 100 MHz for 8-, 16- or 32-bit parallel data and messages, aggregate input bandwidth up to 400 MB/s

Video scaler & de-interlacer unit (MBS)

Scaling	Simultaneous vertical and horizontal scaling with linear and non-linear aspect-ratio conversion
De-interlacing	Simple median, majority-selection (i.e. best of three algorithms), simple field insertion and line doubling, or high-end, NXP edge-dependent de-interlacing (EDDI) algorithm
Filtering	Programmable up to 6-tap polyphase filters
Color/Formats	Variable color space conversion; conversions between 4:2:0, 4:2:2 and 4:4:4; color-key and alpha processing
Performance	Up to 157 Mpix/s

Video output unit (QVCP)

Data formats	24- or 30-bit full parallel RGB or YUV, 16- or 20-bit Y and U/V multiplexed data, 8- or 10-bit 656 (full D1, 4:2:2 YUV), 8- or 10-bit 4:4:4 format in 656-style with RGB or YUV
Resolutions	Up to 1920 x 1080 60p
Clock rates	Up to 148 MHz
Functions	2-layer compositing, picture quality improvements, gamma correction, horizontal 10-tap scaling, genlock mode

Fast generic parallel output unit (FGPO)

Data rate	Up to 100 MHz for 8-, 16- or 32-bit parallel data and messages, aggregate output bandwidth up to 400 MB/s

Audio input & output units (AI & AO)

Sample size	8 channels, 16- or 32-bit samples per channel
Sample rates	Programmable with 0.001 Hz resolution; maximum sample rate is application dependent
Data formats	16-bit (mono and stereo), 32-bit (mono and stereo), PC standard memory data format
Clock source	Internal or external
Native protocol	I^2S over serial 6-wire protocols

Specifications (continued)

S/PDIF input & output units (SPDI & SPDO)

Sample size	6 channels,16 or 24 bits per channel
Bit rate	Up to 40 Mbits/s in raw mode
Native protocol	IEC-958, 1 wire

2D drawing engine

Functions	Solid fills, 3-operand bitblt, lines, monochrome data expansion, 256-level alpha bitblt (to blend 2 images), anti-aliased lines and fonts
Formats	8-, 16-, and 32-bit/pixel

Variable length decoder unit (VLD)

Functions	Parses MPEG-1 and MPEG-2 elementary bitstreams generating run-level pairs and filling macroblock headers

DVD descrambler unit (DVDD)

Functions	Authentication, descrambling

I²C interface

Modes	Master and slave
Addressing	Up to 10-bit
Speed	*standard* 100 kHz *fast* 400 kHz

Ethernet MAC

Interface	10/100 IEEE 802.3, MII, and RMII
Functions	Real-time traffic, QoS

PCI/XIO bus interface

Width	32-bit data, 32-bit address space
Speed	33-MHz PCI 2.2 interface with integrated PCI bus arbiter up to 4 masters
Voltage	3.3 V (5 V tolerant)
Functions	PCI master and slave 8-, and 16-bit NAND or NOR Flash memories IDE controller

Memory system

Speed	Up to 200 MHz (1.6 GB/s)
Memory size	8 to 256 MB
Supported types	64 to 512 Mbit DDR SDRAM devices
Width	16- or 32-bit bus
Signal levels	2.5 V SSTL-II

Timers

Number	8
Sources	(prescaled) CPU clock, data or instruction breakpoints, cache events, video I/O clocks, audio in/out word strobe

GPIO

Dedicated pins	16
Functions	Software I/O, external interrupt, universal RC blaster, clock source/gate for system event timers/ counters, emulating high-speed serial protocols

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